Ujwal R. Shirode

ASSISTANT PROFESSOR

Department of Electronics and Telecommunication

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ACADEMIC BACKGROUND

- **M.Tech** (VLSI Technology) in 2013 from **Electronics and Engineering Department** of **North Maharashtra University** with first class.
- **B. E in 2010** (Electronics and Telecommunication) from **SSBT'S College of Engineering** with Distinction.

AREA OF INTERESTS

- RTL coding of digital circuits in VHDL/VERILOG and in System Verilog.
- Verification modeling/Test bench coding in VERA , System C and in System Verilog.
- ASIC Design (Front End Design).
- FPGA Development.
- Object Oriented Programing Using C++ , JAVA and System Verilog.
- Developing and Designing Data Structures and Algorithms.
- Scripting in Unix, Linux and in TCL.
- CMOS level Designing.
- Static Timing Analysis(STA) in VLSI design.
- Developing and handling EDA Tools.

WORK EXPERIENCE

- Currently working with **PCCOE, Pune** as an Assistant Professor (since June 2014)
- 1 years of experience in the field of **Software Developer** with Cognizant Technology.
- 6 months of experience with **Nano Science Lab, Hyderabad as a Physical Design Trainee**

Subjects Taught

- System Programming and Operating Systems
- Antenna and Wave Propagation Theory

Other Information

- Number of paper published in International Journals : 2
- Number of Patents : 6

Personal Details

Name : Ujwal Ramesh Shirode

Address : 52/a, Shastri Nagar, Near Girna Tank, Jalgaon-425002

Date of Birth : 18/05/1989